INDIVIDUAL FACULTY PROFILE- TEMPLATE TO BE UPLOADED IN COLLEGE WEBSITE

<table>
<tr><td>  </td><td>Name in Caps: Dr. R.JAYAGOWRI
Designation: Associate professor
Qualification: Ph.d
Email-id: (official): rjayagowri.ece@bmsce.ac.in
Experience: 22yrs
Teaching experience: 22yrs
Date of Joining this Institution (BMSCE): 18.8.2014

<u>Research Interests:</u>
ASIC Design, Design for Testability, low power IC design, Physical design, Static Timing Analysis.</td></tr>
<tr><td>About Your self</td><td>Paragraph (Minimum 10 Lines) –
Completed the B.E degree from Bharathidasan university, Trichy in Electronics and Communication Engineering. Obtained the M.E degree in Applied Electronics from college of Engineering, Guindy, Anna university, Guindy, Chennai. Obtained the Ph.d in power optimization technique for design for testability from Jawaharlal Nehru technological university, Hyderabad.

Having teaching experience of 22 years by working in different organization like VIT, Vellore, RV-VLSI, KS institute of Technology etc... Taught different subjects in the domain of VLSI, also trained the corporate freshers from NXP semiconductors and Honeywell for ASIC design.

Authored two books in the field of VLSI titled as “Static Timing Analysis for VLSI circuits” and “Analog and Mixed mode VLSI design”. Published more than 30 technical research papers in International and national journals and conferences which includes (IEEE and Springer publications).

As an achievement won the Best teacher award, best technical paper award. Along with students won the “Winner award in bachelor category in All India cadence design contest -2012”, “Project of the year-Karnataka-2012” award, “Top 7 of national category- bachelor level cadence design contest-2013”.</td></tr>
<tr><td></td><td><u>Education:</u>
Doctoral Research: Ph.d(Engg) in VLSI- low power in Design for Testability from Jawaharlal Nehru Technological University, Hyderabad.
Masters: M.E, College of engineering guindy, Anna university, Guindy, Chennai.
Bachelors:B.E, Bharathidasan University, Trichy
Other Degree/Diploma/PG diploma if any</td></tr>
<tr><td></td><td>Personal web site/page if any then mention the Webpage link</td></tr>
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	Selected Publications **(Year wise)** • Bhavana Adiga H P, R. Jayagowri "Application of Quantum Cellular Automata in Image Steganography with an Improved Fault Tolerant Majority Voter", 2018 ***3rd IEEE International Conference on Recent Trends in Electronics, Information & Communication Technology*** (RTEICT-2018), MAY 18th & 19th 2018 • Sujatha masillamani, R.Jayagowri "A review on Hybrid SOC", 2018 ***IEEE International Conference on Current trends towards Converging Technologies*** *(ICCTCT 2018)*, March-2018. • Shanthala .L , Jayagowri .R ; "Efficient Timing Closure in SOC through Timing Quality Checks and Engineering Change Order" published in ***International Journal of Advance Research, Ideas and Innovations in Technology, (Volume3, Issue3)*** May-2017, Page | 699-705, ISSN: 2454-132X • Shanthala .L , Jayagowri .R ; "Simultaneous Data Path and Clock Path Engineering Change Order for Efficient Timing Closure in Complex SOC", published in ***IOSR Journal of VLSI and Signal Processing (IOSR-JVSP) Volume 7, Issue 3, Ver. I*** (May. - June. 2017), PP 35-41, e-ISSN: 2319 – 4200, p-ISSN No. : 2319 – 4197,DOI: 10.9790/4200-0703013541 **.(Impact factor:2.82)** • Shruti K, R. Jayagowri, "VLSI Architecture of Colour Interpolation Processor for Real Time Video Application Using Adaptive Edge Enhancement Technique", ***International Journal of Electrical Electronics & Computer Science Engineering Special Issue – June 2016 -NEWS 2016*** | E-ISSN : 2348-2273 | P-ISSN : 2454-1222, pp130-135, **P Impact Factor (2016) :3.952** • R. Jayagowri **,** "Techniques for Low Power and Area Optimized VLSI Testing using Novel Scan Flip-Flop" published in ***International Journal of Computer Applications(IJCA) (0975 – 8887), Vol. 113 , No. 5***, March 2015, pp 22- 28. ISBN : 973-93-80885-52-9**. Impact factor 2014: 0.715.** • Vinay S, pramod K. P, R. Jayagowri, S. Ranjana & priyanka V, " Implementation of Low Power VLSI Architecture for Lossless Compressor and Decompressor", published in ***International Journal of Electronics and Communication Engineering(IJECE),*** ISSN(P): 2278-9901; ISSN(E): 2278-991X, Vol. 2, Issue 5, Nov 2013, pp 205-212.**Impact factor(JCC): 3.2029**

	• R. Jayagowri and K. S. Gurumurthy, Gating Technique with Modified Scan Flip-flop for Low Power Testing of VLSI Chips, ***VLSI Design and Test Symposium (VDAT'12)****, July 2012,* ***Springer LNCS 7373*****, pp(52-58)**. • Jayagowri, R., Gurumurthy, K.S : A Technique for Low Power Testing of VLSI Chips. In: Proceedings of ***IEEE International Conference on Devices, Circuits and Systems***, **IEEE DOI: 10.1109/ICDCSyst.2012.6188654**, pp. 662 – 665, March 2012, pp.661-664. • R. Jayagowri, karthik.S.Rao, Karthik.C.V, Keshava Koushik.S , "Design and Implementation of Low-Power Pipelined FFT Processor", Published in ***International Journal of VLSI & Signal Processing Applications***,2012, **ISSN 2231-3133**, Vol-2, Issue-4,pp 330-335. • R. Jayagowri and K. S. Gurumurthy, "Design and Implementation of Area and Power Optimized Novel Scan flop", ***published in International journal of VLSI Design & Communication Systems (VLSICS),*** **ISSN 0976 – 1357**, Vol.2, No.1, March 2011, pp.37-43**. Academic Resources Impact factor:4** • R. Jayagowri and K. S. Gurumurthy, "Power Optimization during Shift Cycle of Scan based IC Testing ",published in the International Journal of Recent Trends in Engineering, by the Academy Publishers, Finland, **ISSN 2158-5555**, Vol.4, No.3, Nov 2010, pp 135-138. • R.Jayagowri: " Low power CMOS Technique implementation for real time image processing architecture", ***International conference on emerging microelectronics and interconnection technology, EMIT-08***, conducted by **IMAPS India chapter** between December 15th to 18th 2008. • Jayagowri, R., C. Meena: " Power efficient technique for C & S unit in image processing Architecture", *National conference on VLSI organised by TPGIT, vellore, Anna university* on 12th August 2006. • Jayagowri, R., Dr. N. Kumaravel: "Feature clustering and labeling for video object segmentation using ANN," *National conference on emerging trends in engineering and technology*, conducted by Dr. M.G.R educational and research institute, Deemed University, between May 1 – May3, 2004. • Jayagowri, R.: " A view of telemedicine ECG, Blood pressure" in *National Seminar electronics advances and trends* conducted by Arunai engineering college between January 23 January 24, 2000.

	• Jayagowri, R., Dr. K. Chidambaram: "Optics a tool for biomedical engineering", *National Seminar on Bio-medical engineering*. The Indian scenario 12th march – 13th march 1999. Organised b center for Bio medical engineering, Vellore Engineering College, between 12th & 13th March 1999.
	Courses Handled/List Static Timing Analysis Low power VLSI Design for Testability Physical Design System Verilog and Verification Digital VLSI design Physical Design automation Hardware description Language Synthesis and optimization of Digital circuits SOC design ASIC Design Fundamentals of VLSI Design Microelectronic circuits Electronic measurements and Instrumentation Elements of Electrical and Electronics Engineering
	Additional Responsibilities **(held in BMSCE)** Board of Examination for ECE department PG Feedback co-coordinator of the department Industry internship co-ordinator for VLSI stream PG project co-ordinator for VLSI stream Co-coordinaor for organizing the GIAN program from ECE department Student Proctor
	Other Information: